



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO.          | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--------------------------|-------------|----------------------|---------------------|------------------|
| 10/729,391               | 12/05/2003  | Yoshifumi Sekiguchi  | 81940.0066          | 9563             |
| 26021                    | 7590        | 01/24/2008           |                     |                  |
| HOGAN & HARTSON L.L.P.   |             |                      | EXAMINER            |                  |
| 1999 AVENUE OF THE STARS |             |                      | SITTA, GRANT        |                  |
| SUITE 1400               |             |                      |                     |                  |
| LOS ANGELES, CA 90067    |             |                      | ART UNIT            | PAPER NUMBER     |
|                          |             |                      | 2629                |                  |
|                          |             |                      |                     |                  |
|                          |             |                      | MAIL DATE           | DELIVERY MODE    |
|                          |             |                      | 01/24/2008          | PAPER            |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| <b>Office Action Summary</b> | <b>Application No.</b> | <b>Applicant(s)</b> |
|------------------------------|------------------------|---------------------|
|                              | 10/729,391             | SEKIGUCHI ET AL.    |
| Examiner                     | Art Unit               |                     |
| Grant D. Sitta               | 2629                   |                     |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 05 December 2003.

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-39 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1,2,12-19 and 21-39 is/are rejected.

7)  Claim(s) 3-11,20 is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 05 December 2003 is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892) 4)  Interview Summary (PTO-413)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date. \_\_\_\_ .  
3)  Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 3/21/00. 5)  Notice of Informal Patent Application  
6)  Other: \_\_\_\_ .

## DETAILED ACTION

### ***Specification***

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

### ***Claim Objections***

2. Claim 19 objected to because of the following informalities: Says "crystal liquid" when "liquid crystal" was intended (claim 19, pg 151, 7 lines from top of claim 19). Appropriate correction is required.

### ***Drawings***

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "vibrate with a vibration center" (claims 22, 23, and 24) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 22-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by "vibrate with a vibration center" (claims 22, 23, and 24).

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 12, 13, 15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Murakami et al (6,040,814) hereinafter, Murakami.

8. In regards to claim 1, Murakami teaches a method of driving an active-matrix liquid-crystal display (“active-matrix LCD” abstract) device including a liquid-crystal panel comprising (fig. 1 (1)): a pair of substrates (col. 5, line 8), at least one of which is a transparent substrate; a plurality of data lines (fig. 1 (12)), which are each extended in a row direction on a specific one of said substrates and are arranged in a column direction perpendicularly intersecting said row direction (fig. 1 (12) and col. 5, lines 1-18); a plurality of gate lines (fig. 1 (13)), which are each extended in said column direction and are arranged in said row direction (fig. 1 (13) and col. 5 lines 1-18); an active device (fig. 1 (TFT)) connected at an intersection of each of said data lines (fig. 1 (12)) and each of said gate lines (fig. 1 (13)); a pixel electrode (fig. 1 (C)) driven by said active device (fig. 1 (TFT)); an opposite electrode provided on said specific substrate or the other one of said substrates as an electrode sandwiching (fig. 7B (17)) a liquid-crystal layer between said opposite electrode and said pixel electrode (col. 5, lines 20-

36)) ; and a storage capacitor connected in parallel to said liquid-crystal layer (fig. 3 (CLC)); wherein:

a frame period of an image displayed on said liquid-crystal panel is divided into a scanning period and a hold period (fig. 6B "WRITE PERIOD" and "SUSTAIN PERIOD") longer than said scanning period (fig. 6b the sustain period is longer than the write period); in said scanning period, image data of an amount corresponding to a frame (fig. 6b (1H)) is written into said liquid-crystal panel (fig. 1 (1)); in said hold period following said scanning period (fig. 6b Vcom), an off state is sustained (fig. Fig. 6b V1,V2, V3 and V4); an electric potential appearing on a positive-polarity data line in said hold period is increased to a level higher than an electric potential appearing on said opposite electrode (fig. 6B (V1, V2, V3, and V4 both polarities) where said positive-polarity data line is defined as said data line, on which an electric potential appears at a level higher than an electric potential (col. 6-7, lines 66-64 "In FIG. 6B, data voltages applied to the data line n increase from V0step by step, and the absolute values of data voltages applied to the data lines n+1 and n+2 are unchanged. Data voltages applied to the data line n+3 are opposite to those applied to the data line n.") appearing on said opposite electrode when an electric potential appearing on said gate line changes from an on-state level to an off-state level in said scanning period; and an electric potential appearing on a negative-polarity (col. 6, lines 23-28 "active-matrix LCD and shows signed voltages to be stored in the cells of the LCD. To prevent flickering, the polarities of voltages applied to the cells are alternated column by column (fig. 4 + and - V), or row by row, or both. The polarity of a voltage applied to a given cell is changed frame by

frame") data line in said hold period is decreased to a level lower than said electric potential appearing on said opposite electrode where said negative-polarity data line (fig. 8 (data line voltage and sustained voltage) is defined as said data line provided on a row adjacent to said positive-polarity data (col. 8-10, lines 15- 10) line as said data line , on which an electric potential appears at a level lower than an electric potential appearing on said opposite electrode (fig. 20, Data voltage and polarity control) when an electric potential appearing on said gate line changes from an on-state level to an off-state level in said scanning period (fig. 8 col. 8 lines 15-67 and fig. 3b and col. 5-6, lines 20-65).

9. In regards to claim 13, Murakami teaches a method of driving an active-matrix liquid-crystal display ("active-matrix LCD" abstract) device including a liquid-crystal panel comprising (fig. 1 (1)): a pair of substrates (col. 5, line 8), at least one of which is a transparent substrate; a plurality of data lines (fig. 1 (12)), which are each extended in a row direction on a specific one of said substrates and are arranged in a column direction perpendicularly intersecting said row direction (fig. 1 (12) and col. 5, lines 1-18); a plurality of gate lines (fig. 1 (13)), which are each extended in said column direction and are arranged in said row direction (fig. 1 (13) and col. 5 lines 1-18); an active device (fig. 1 (TFT)) connected at an intersection of each of said data lines (fig. 1 (12)) and each of said gate lines (fig. 1 (13)); a pixel electrode (fig. 1 (C)) driven by said active device (fig. 1 (TFT)); an opposite electrode provided on said specific substrate or the other one of said substrates as an electrode sandwiching (fig. 7B (17)) a liquid-crystal layer between said opposite electrode and said pixel electrode (col. 5, lines 20-

36)) ; and a storage capacitor connected in parallel to said liquid-crystal layer (fig. 3 (CLC)); wherein:

a frame period of an image displayed on said liquid-crystal panel is divided into a scanning period and a hold period (fig. 6B "WRITE PERIOD" and "SUSTAIN PERIOD") longer than said scanning period (fig. 6b the sustain period is longer than the write period); in said scanning period, image data of an amount corresponding to a frame (fig. 6b (1H)) is written into said liquid-crystal panel (fig. 1 (1)); in said hold period following said scanning period (fig. 6b Vcom), an off state is sustained (fig. Fig. 6b V1,V2, V3 and V4); and said liquid-crystal display device includes a scanning-period electric-potential control means (fig. 1 (4)) for controlling an electric potential in said hold period (col. 5 line 1-20); and wherein: said scanning-period electric-potential control means increases an electric potential appearing on a positive-polarity data line (fig. 4 odd and even) in said hold period to a level higher than an electric potential appearing on said opposite electrode where said positive-polarity data line is defined as said data line (col. 8, lines 15-67), on which an electric potential appears at a level higher than an electric potential appearing on said opposite electrode when an electric potential appearing on said gate line changes from an on-state level to an off-state level in said scanning period ("The fourteenth embodiment forms a capacitor Cs in each cell and an auxiliary line connected to the capacitor Cs. The capacitor Cs serves as a sustain capacitor of a cell electrode. When a TFT of each cell is of an n-channel type, a direct-current component of a voltage on the auxiliary line during a period Toff-data is set to be higher than a voltage on the auxiliary line just before a voltage on a scan line changes from Vgon to

Vgoff in a period Ton-data. By adjusting the voltage of the auxiliary line during the periods Ton-data and Toff-data and by using the capacitive dividing function of the capacitor Cs and other capacitors of each cell electrode, the voltage level of the cell electrode during the period Toff-data can be precisely controlled" col. 21-22, lines 53-36); and said scanning-period electric-potential control means (fig. 1 (4)) decreases an electric potential appearing on a negative-polarity data line (fig. 4 (column n+1)) in said hold period to a level lower (col. 21-22, lines 53-36) than said electric potential appearing on said opposite electrode where said negative-polarity data line is defined as said data line provided on a row adjacent to said positive-polarity data line as said data line (col. 8, lines 15-67), on which an electric potential appears at a level lower than an electric potential appearing on said opposite electrode when an electric potential appearing on said gate line changes from an on-state level to an off-state level in said scanning period (col. 6, lines 30-50).

10. In regards to claim 2, Murakami teaches wherein said electric potential appearing on said positive-polarity data line in said hold period is set at a fixed level higher than said electric potential appearing on said opposite electrode and said electric potential appearing on said negative-polarity data line in said hold period is set at a fixed level lower than said electric potential appearing on said opposite electrode (fig. 4 and fig. 8 col. 8, lines 15-67).

11. In regards to claim 12, Murakami teaches a method of driving an active-matrix liquid-crystal display device according to claim 1 wherein, as said electric potential appearing on said data line in said hold period: said electric potential appearing on said positive-polarity data line in said hold period is set at a level minimizing a change of a transmittance or a reflectance of a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively in a positive-polarity frame period of said pixel connected to a specific one of said scanning lines, which is close to the last one of said gate lines; and said electric potential appearing on said negative-polarity data line in said hold period is set at a level minimizing a change of a transmittance or a reflectance of a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively in a negative-polarity frame period of said pixel connected to a specific one of said scanning lines, which is close to the last one of said gate lines (col. 6-7, lines 59-61).

12. In regards to claim 15, Murakami teaches said active device provided is a thin-film transistor (fig. 1 TFT); and said thin-film transistor provided for a pixel is located in a middle location between a specific one of said data lines and an adjacent one of said data lines where said specific data line is defined as a data line connected to a source of said thin-film transistor and said adjacent data line is defined as a data line located on

a pixel side opposite to said specific data line to sandwich said pixel between said adjacent data line and said specific data line (fig. 3a TFT, n and n+1).

13. In regards to claim 17, Murakami teaches said active device is a thin film transistor (fig. 1 TFT)); pixels are arranged to form an N.times.M matrix comprising N rows and M columns; and said matrix includes a portion in which, if a source of said thin-film transistor provided for a specific pixel located at an intersection of the nth row and mth column of said matrix is connected to one of two data lines adjacent to said pixel where n is an integer in the range 1 to (N-1) and m is an integer in the range 1 to M, a source of a thin-film transistor provided for a pixel located at an intersection of the (n+1)th row and said mth column is connected to one of said two adjacent data lines, which is not connected to said source of said thin-film transistor provided for said specific pixel (fig. 3a n, n+1, 12, 13 and TFT).

***Claim Rejections - 35 USC § 103***

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claims 14, 16, 18, 19, 21, 22, 24-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami, in view of Yatabe et. al (US 6,940,484) hereinafter, Yatabe.

17. In regards to claim 14, Murakami discloses the limitations of claim 13, Murakami differs from the claimed invention in that Murakami does not disclose wherein the gate-line scanning circuit includes shift registers.

However, Yatabe teaches a system and method for a gate-line-scanning circuit for scanning said gate lines; wherein: said gate-line-scanning circuit includes a shift register for selecting any of said gate lines, and said shift register includes a spare register for putting all said gate lines in an off state. ( "FIG. 6 is a block diagram showing the configuration of this Y driver 350. In this figure, a shift register 3502 is a 200-bit shift register which corresponds to the total number of scanning lines 312, shifts a start pulse YD supplied at the beginning of one frame according to clock signals YCLK having" col. 13, lines 8-23)

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Murakami to include the use of shift registers as taught by Yatabe in order to shift the pulse through out the scan lines.

18. In regards to claim 16, Yatabe teaches active device is a thin-film transistor; and in said pixel electrode for a pixel, an electrode portion made of a reflective material having electro conductivity is provided at such a location that said thin-film transistor for said pixel is positioned at a center of said electrode portion made of a reflective material having electro conductivity (col. 24, lines 21-35).

19. In regards to claim 18, Murakami teaches if the number of said data lines is  $(M+1)$ , said data line on the first column is connected to said data line on the  $(M+1)$ th column (fig. 32 column 1 and column 3 are connected through VD).

20. In regards to claim 19, Murakami teaches a method of driving an active-matrix liquid-crystal display device in accordance with claim 2 wherein:

    said fixed electric potential appearing on said positive-polarity data line in said hold period is set at a level higher than a sum ( $V_{com}+V_p$ ) of an electric potential  $V_{com}$  appearing on said opposite electrode and an absolute value  $V_p$  of a voltage appearing on said crystal liquid for a positive polarity defined as a polarity for which an electric

potential appearing on said pixel electrode is higher than an electric potential appearing on said opposite electrode facing said pixel electrode to provide a gap for sandwiching said liquid-crystal layer with a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively among transmittance or reflectance values in a range of voltages appearing on said liquid crystal as voltages used in a display (fig. 6b VD (n+2); and

    said fixed electric potential appearing on said negative-polarity data line in said hold period is set at a level lower than a sum (Vcom-Vm) of said electric potential Vcom and an absolute value Vm of a voltage appearing on said crystal liquid for a negative polarity defined as a polarity for which an electric potential appearing on said pixel electrode is lower than an electric potential appearing on said opposite electrode facing said pixel electrode to provide a gap for sandwiching said liquid-crystal layer with a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively among transmittance or reflectance values in said range of voltages appearing on said liquid crystal as voltages used in a display (fig. 6b (VD (n+1)).

21. In regards to claim 21, Murakami teaches said fixed electric potential appearing on said positive-polarity data line in said hold period is set at a level higher than Vsp50 and said fixed electric potential appearing on said negative-polarity data line in said hold period is set at a level lower than Vsm50, where: (fig. 6b (VD (n+1)) symbol Vsp50

denotes an electric potential appearing on said positive-polarity data line as an electric potential corresponding to a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively among transmittance or reflectance values in a range of voltages appearing on said liquid crystal as voltages used in a display (fig. 6b VD (n+2) ); and symbol Vsm50 denotes an electric potential appearing on said negative-polarity data line as an electric potential corresponding to a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively among transmittance or reflectance values in said range of voltages appearing on said liquid crystal as voltages used in a display (col. 6-7, lines 67-45).

22. In regards to claim 22, Murakami teaches a method of driving an active-matrix liquid-crystal display device according to claim 1 wherein: said electric potential appearing on said positive-polarity data line in said hold period is driven to vibrate with a vibration center coinciding with a level higher than a sum (Vcom+Vp) of an electric potential Vcom appearing on said opposite electrode and an absolute value Vp of a voltage appearing on said crystal liquid for a positive polarity defined as a polarity for which an electric potential appearing on said pixel electrode is higher than an electric potential appearing on said opposite electrode facing said pixel electrode to provide a gap for sandwiching said liquid-crystal layer with a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance

respectively among transmittance or reflectance values in a range of voltages appearing on said liquid crystal as voltages used in a display (fig. 6b (VD (n+1))).

and said electric potential appearing on said negative-polarity data line in said hold period is driven to vibrate with a vibration center coinciding with a level lower than a sum (Vcom-Vm) of said electric potential Vcom and an absolute value Vm of a voltage appearing on said crystal liquid for a negative polarity defined as a polarity for which an electric potential appearing on said pixel electrode is lower than an electric potential appearing on said opposite electrode facing said pixel electrode to provide a gap for sandwiching said liquid-crystal layer with a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively among transmittance or reflectance values in said range of voltages appearing on said liquid crystal as voltages used in a display (fig. 6b (VD (n+1))).

23. In regards to claim 24, Murakami teaches: said electric potential appearing on said positive-polarity data line in said hold period is driven to vibrate with a vibration center coinciding with a level higher than Vsp50 and said electric potential appearing on said negative-polarity data line in said hold period is driven to vibrate with a vibration center coinciding with a level lower than Vsm50, (fig. 6b (VD (n+1)) and (fig. 6b (VD (n+1))) where: symbol Vsp50 denotes an electric potential appearing on said positive-polarity data line as an electric potential corresponding to a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a

maximum reflectance respectively among transmittance or reflectance values in a range of voltages appearing on said liquid crystal as voltages used in a display; and symbol Vsm50 denotes an electric potential appearing on said negative-polarity data line as an electric potential corresponding to a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively among transmittance or reflectance values in said range of voltages appearing on said liquid crystal as voltages used in a display .

24. In regards to claim 25, Murakami teaches said fixed electric potential appearing on said positive-polarity data line in said hold period and said fixed electric potential appearing on said negative-polarity data (fig. 5a V2n –V2 (n+1)) line in said hold period are set at such values that an absolute value of a difference between said fixed electric potential appearing on said positive-polarity data line and an electric potential appearing on said opposite electrode is approximately equal to an absolute value of a difference between said fixed electric potential appearing on said negative-polarity data line and said electric potential appearing on said opposite electrode (col. 6, lines 30-58).

25. In regards to claim 26, Murakami teaches wherein said fixed electric potential appearing on said positive-polarity data line in said hold period and said fixed electric potential appearing on said negative-polarity data line in said hold period are set at such values that an absolute value of a difference between said fixed electric potential

appearing on said positive-polarity data line (fig. 8 (1H)) and a data-line center electric potential is approximately equal to an absolute value of a difference between said fixed electric potential appearing on said negative-polarity data line and said data-line center electric potential where said data-line center electric potential is defined as a center electric potential between maximum and minimum values of electric potentials each appearing on said data lines as an electric potential used in a display (col. 6, lines 30-58).

26. In regards to claim 27, Murakami teaches wherein a parasite capacitance between said pixel electrode and one of two data lines adjacent to said pixel electrode is approximately equal to a parasite capacitance between said pixel electrode and the other one of said data lines adjacent to said pixel electrode (figs 9a and 9b col. 9, lines 4-35 "FIGS. 9A and 9B explain the principle of a correction according to the first aspect of the present invention, in which FIG. 9A shows parasitic capacitors formed between a cell and adjacent data and scan lines, and FIG. 9B explains the correction. This correction considers only the parasitic capacitors formed between a given cell and adjacent data and scan lines. There are other parasitic capacitors formed between the cell and other data and scan lines, and they also must be considered if they are not ignorable. For the sake of simplicity, this embodiment considers only the parasitic capacitors formed between a given cell and adjacent data and scan lines.").

27. In regards to claim 28, Murakami teaches wherein a horizontal period of a scanning period of a frame includes a period for setting said electric potential appearing on said data line at any arbitrary level in addition to a period for setting said electric potential appearing on said data line at a level corresponding to desired image data (fig. 6b write and sustain period col. 6-7, lines 59-61).

28. In regards to claim 29, Murakami teaches wherein said period for setting said electric potential appearing on said data line at any arbitrary level is a period during which said positive-polarity data line is short-circuited to said negative-polarity data line (col. 5-6, lines 48-12 "When the TFT is of an n-channel type, the data driver 2 and scan driver 3 apply the data voltage and scan pulse shown FIG. 3B to the data line 12 and scan line 13, respectively. In response to an instruction signal, the data driver 2 applies data voltages to the data lines, respectively. The scan driver 3 applies the scan pulse sequentially to the scan lines. When the positive scan pulse is applied to a given scan line 13, the TFTs of cells connected to the scan line are turned on to connect the cell electrodes of the cells to the data lines 12, respectively. Then, the cells receive data voltages applied to the data lines 12 and are charged thereby. When the scan pulse disappears to turn off the TFTs, the cells sustain the data voltages until the next scan pulse is applied to the corresponding scan line. The time required to write display data to a full screen of the LCD is called a frame, and every scan line receives a scan pulse

frame by frame. Namely, the cells connected to a given scan line are written frame by frame.").

29. In regards to claim 30, Murakami teaches wherein said period for setting said electric potential appearing on said data line at any arbitrary level is a period during which said positive-polarity data line, said negative-polarity data line, said opposite electrode and said storage line are short-circuited to each other (fig. 6b write and sustain period col. 6-7, lines 59-61 and (col. 5-6, lines 48-12).

30. In regards to claim 31, Murakami teaches wherein said period for setting said electric potential appearing on said data line at any arbitrary level is a period during which said electric potential appearing on said data line is set at a level equal to or lower than said electric potential appearing on said opposite electrode in a case where said data line is said positive-polarity data line or a level equal to or higher than said electric potential appearing on said opposite electrode in a case where said data line is said negative-polarity data line (col. 6, lines 30-58).

In regards to claim 32, Murakami teaches wherein said period for setting said electric potential appearing on said data line at any arbitrary level is a period during which said electric potential appearing on said data line is set at said electric potential appearing on

said negative-polarity data line in said hold period in a case where said data line is said positive-polarity data line or at said electric potential appearing on said positive-polarity data line in said hold period in a case where said data line is said negative-polarity data line (fig. 6b write and sustain period).

31. In regards to claim 33, Murakami teaches wherein said period for setting said electric potential appearing on said data line at any arbitrary level is a period during which said electric potential appearing on said data line is set at a minimum value of said electric potentials each appearing on said data line as an electric potential used in a display in a case where said data line is said positive-polarity data line or at a maximum value of said electric potentials each appearing on said data line as an electric potential used in a display in a case where said data line is said negative-polarity data line (fig. 8 polarity signal and sustained voltage signal).

32. In regards to claim 34, Murakami teaches a horizontal period of a scanning period of a frame includes a specific period for setting all said gate lines in an off state and setting said electric potential appearing on said data line at any arbitrary level in addition to a period for setting said electric potential appearing on said gate line at an on-state level, setting said electric potential appearing on said data line at a level for writing desired image data and applying an electric potential for writing said desired image data to said pixel electrode; and one or more said specific periods are provided in

said scanning period before said image data is written into a pixel connected to a last gate line (fig. 9a fig. 10 write scan line and Vg on, col. 10, lines 18-38)).

33. In regards to claim 35, Murakami teaches wherein said specific period for setting said electric potential appearing on said data line at any arbitrary level is a period during which said electric potential appearing on said data line is set at a level equal to or lower than said electric potential appearing on said opposite electrode in a case where said data line is said positive-polarity data line or a level equal to or higher than said electric potential appearing on said opposite electrode in a case where said data line is said negative-polarity data line (col. 6, lines 30-58).

34. In regards to claim 36, Murakami teaches wherein said specific period for setting said electric potential appearing on said data line at any arbitrary level is a period during which an absolute value of a difference between said fixed electric potential appearing on said positive-polarity data line and an electric potential appearing on said opposite electrode is approximately equal to an absolute value of a difference between said fixed electric potential appearing on said negative-polarity data line and said electric potential appearing on said opposite electrode (col. 6, lines 30-58).

35. In regards to claim 37, Murakami wherein said specific period for setting said electric potential appearing on said data line at any arbitrary level is a period during which said electric potential appearing on said data line is set at said electric potential appearing on said negative-polarity data line in said hold period in a case where said data line is said positive-polarity data line or at said electric potential appearing on said positive-polarity data line in said hold period in a case where said data line is said negative-polarity data line.

36. In regards to claim 38, Murakami teaches wherein said specific period for setting said electric potential appearing on said data line at any arbitrary level is a period during which said positive-polarity data line is short-circuited to said negative-polarity data line (fig. 8 data line voltage).

37. In regards to claim 39, Murakami teaches wherein said specific period for setting said electric potential appearing on said data line at any arbitrary level is a period during which said positive-polarity data line, said negative-polarity data line, said opposite electrode and said storage line are short-circuited to each other (fig. 6b write and sustain period col. 6-7, lines 59-61 and (col. 5-6, lines 48-12).

***Allowable Subject Matter***

38. Claim 23 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

39. Claims 3,4,5,6,7,8,9,10,11 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

40. The claimed prior art has failed to teach Applicant's claimed invention:

3. A method of driving an active-matrix liquid-crystal display device according to claim 1 wherein said electric potential  $V_{sig}$  [V] appearing on said positive-polarity data line in said hold period has a value in a range expressed in an MKSA unit system by relation (1) as follows:  $12 V_{opt} - [1 + R_{off} R_1] V_c (f) 1 - 1 f V_{sig} V_{opt} + [1 + R_{off} R_1] V_c (f) 1 - 1 f (1)$  where symbol  $\tau$  denotes a quantity expressed by the following equation:  $13 = R_1 R_{off} R_1 + R_{off} (C_1 + C_{sig} + C_{sd})$ , symbol  $V_{opt}$  denotes an electric potential expressed by Eq. (2) as follows:  $14 V_{opt} = V_{com} + (1 + R_{off} R_1) (V_{fst} - V_{com}) (2)$  symbol  $R_{off}$  denotes a resistance [.OMEGA.] exhibited by said active device when said active device is put in an off state; symbol  $R_1$  denotes a resistance [.OMEGA.] exhibited by said liquid-crystal layer sandwiched by said pixel electrodes and said opposite electrode as a resistance expressed by the following equation:  $15 R_1 = d S_{lc}$  symbol  $S$  denotes the area [ $m^{sup.2}$ ] of said pixel electrode; symbol  $d$  denotes the thickness [m] of said liquid-crystal layer; symbol  $\rho_{lc}$  denotes the resistivity [.OMEGA.m] of a liquid crystal composing said liquid-crystal layer; symbol

Vcom denotes said electric potential [V] appearing on said opposite electrode; symbol f denotes a frame frequency [Hz]; symbol Cl denotes the capacitance [F] of said liquid crystal of said liquid-crystal layer; symbol Cstg denotes the capacitance [F] of said storage capacitor; symbol Csd denotes the capacitance [F] of a parasitic capacitor existing between said pixel electrode and said data line for said pixel electrode; symbol Vfst denotes an electric potential [V] appearing on said pixel electrode right after an on-state period in said frame period of said pixel; symbol .DELTA.Vc(f) denotes a change [V] in critical electric potential for said frame frequency f and said electric potential Vfst appearing on said pixel electrode right after said on-state period; symbol Vopt denotes an optimum electric potential [V] with said electric potential Vfst of said pixel electrode held as it is; and symbol Vsig denotes an electric potential Vsig [V] appearing on said positive-polarity data line in said hold period.

4. A method of driving an active-matrix liquid-crystal display device in accordance with claim 3 wherein a value of Vfst used in said Eq. (2) is set at (Vcom+Vop) in determining a range of possible values for said electric potential appearing on said positive-polarity data line or (Vcom-Vom) in determining a range of possible values for said electric potential appearing on said negative-polarity data line where: symbol Vop denotes an absolute value of an electric potential, which appears on said positive-polarity data line when a change of a transmittance or a reflectance of said liquid-crystal panel reaches a maximum accompanying a change of said voltage appearing on said liquid crystal in a range of voltages appearing on said liquid crystal as voltages used in a display; and symbol Vom denotes an absolute value of an electric potential, which

appears on said negative-polarity data line when a change of said transmittance or said reflectance of said liquid-crystal panel reaches a maximum accompanying a change of said voltage appearing on said liquid crystal in said range of voltages appearing on said liquid crystal as voltages used in a display.

5. A method of driving an active-matrix liquid-crystal display device in accordance with claim 3 wherein: in determining a range of possible values for said electric potential appearing on said positive-polarity data line, the value of  $V_{fst}$  used in Eq. (2) is set at said electric potential appearing on said pixel electrode right after said on-state period as an electric potential corresponding to image data of a tone adjacent to a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively in a positive-polarity frame period comprising a specific one of said scanning periods and said hold period following said specific scanning period where said specific scanning period is a period in which said electric potential appearing on said data line is set at a level higher than said electric potential appearing on said opposite electrode when an electric potential appearing on said gate line changes from an on-state level to an off-state level in said scanning period; and in determining a range of possible values for said electric potential appearing on said negative-polarity data line, the value of  $V_{fst}$  used in Eq. (2) is set at said electric potential appearing on said pixel electrode right after said on-state period as an electric potential corresponding to image data of a tone adjacent to a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively in a negative-polarity frame period comprising a

specific one of said scanning periods and said hold period following said specific scanning period where said specific scanning period is a period in which said electric potential appearing on said data line is set at a level lower than said electric potential appearing on said opposite electrode when an electric potential appearing on said gate line changes from an on-state level to an off-state level in said scanning period.

6. A method of driving an active-matrix liquid-crystal display device according to claim 1 wherein: said electric potential  $V_{sig}$  [V] appearing on said positive-polarity data line in said hold period is set at approximately a value expressed in an MKSA unit system by Eq. (3) as follows:  $16 V_{sig} = V_{com} + [1 + R_{off} 1 c d s] .times. V_0 (3)$  and said electric potential  $V_{sig}$  [V] appearing on said negative-polarity data line in said hold period is set at approximately a value expressed in an MKSA unit system by Eq. (4) as follows:  $17 V_{sig} = V_{com} - [1 + R_{off} 1 c d s] .times. V_0 (4)$  where symbol  $V_0$  denotes an absolute value [V] of a voltage appearing on said liquid crystal as a voltage corresponding to any arbitrary image data.

7. A method of driving an active-matrix liquid-crystal display device in accordance with claim 6 wherein, when an electric potential appearing on a gate line in a scanning period of a frame period has been set at an on-state level, said electric potential appearing on said data line has been set at a level for writing desired image data and, right after that, all said gate lines have been put in an off state, desired image data is written into all said pixels by carrying out driving repeatedly on each of said gate lines to: set said electric potential appearing on said data line, which serves as said positive-

polarity data line, at a level symmetrical with respect to an electric potential appearing on said positive-polarity data line in said on-state period with its center of symmetry coinciding with a data-line electric potential approximately equal to a quantity expressed by said Eq. (3); and set said electric potential appearing on said data line, which serves as said negative-polarity data line, at a level symmetrical with respect to an electric potential appearing on said negative-polarity data line in said on-state period with its center of symmetry coinciding with a data-line electric potential approximately equal to a quantity expressed by said Eq. (4).

8. A method of driving an active-matrix liquid-crystal display device in accordance with claim 6 wherein: driving is carried out on  $k$  gate lines of said gate lines to set said electric potentials appearing on said  $k$  gate lines in said scanning period of said frame period at an on-state level, set said electric potential appearing on said data line at levels for writing pieces of desired picture data and write said electric potentials corresponding to said pieces of desired image data into said pixel electrodes; right after that, all said gate lines are put in an off state; and desired picture data is written into all said pixels by carrying out driving repeatedly on each of said  $k$  gate lines to: set each of  $k$  electric potentials appearing on said data line, which serves as said positive-polarity data line, at a level approximately symmetrical with respect to an electric potential appearing on said positive-polarity data line in a period of scanning said  $k$  gate lines as one of  $k$  electric potentials each corresponding to one of said  $k$  pieces of desired image data for an arbitrary period length with its center of symmetry coinciding with a data-line electric potential equal to a quantity expressed by said Eq. (3); and set each of  $k$  electric

potentials appearing on said data line, which serves as said negative-polarity data line, at a level approximately symmetrical with respect to an electric potential appearing on said negative-polarity data line in a period of scanning said  $k$  gate lines as one of  $k$  electric potentials each corresponding to one of said  $k$  pieces of desired image data for an arbitrary period length with its center of symmetry coinciding with a data-line electric potential equal to a quantity expressed by said Eq. (4).

9. A method of driving an active-matrix liquid-crystal display device in accordance with claim 6 wherein: driving is carried out on  $k$  gate lines of said gate lines to set said electric potentials appearing on said  $k$  gate lines in said scanning period of said frame period at an on-state level, set said electric potential appearing on said data line at levels for writing pieces of desired image data and write said electric potentials corresponding to said pieces of desired data into said pixel electrodes; right after that, all said gate lines are put in an off state; and desired image data is written into all said pixels by carrying out driving repeatedly on each of said  $k$  gate lines to: set said electric potential appearing on said data line, which serves as said positive-polarity data line, at a level approximately symmetrical with respect to an average of electric potentials appearing on said positive-polarity data line in a period of scanning said  $k$  gate lines as  $k$  electric potentials each corresponding to one of said  $k$  pieces of desired data with its center of symmetry coinciding with a data-line electric potential equal to a quantity expressed by said Eq. (3); and set said electric potential appearing on said data line, which serves as said negative-polarity data line, at a level approximately symmetrical with respect to an average of electric potentials appearing on said negative-polarity data

line in a period of scanning said k gate lines as k electric potentials each corresponding to one of said k pieces of desired image data with its center of symmetry coinciding with a data-line electric potential equal to a quantity expressed by said Eq. (4).

10. A method of driving an active-matrix liquid-crystal display device in accordance with claim 6 wherein a quantity represented by symbol  $V_o$  in Eqs. (3) and (4) as the absolute value of said voltage appearing on said liquid crystal is set at a magnitude equal to about an effective value of said liquid-crystal voltage for which a change in transmittance or reflectance reaches a maximum accompanying a change of said voltage appearing on said liquid crystal as a voltage used in a display.

11. A method of driving an active-matrix liquid-crystal display device in accordance with claim 6 wherein: a quantity represented by symbol  $V_o$  in Eq. (3) as the absolute value of said voltage appearing on said liquid crystal is set at the absolute value of said voltage appearing on said liquid crystal for a positive polarity for which a transmittance or a reflectance of said liquid-crystal display device is equal to about half a maximum transmittance or a maximum reflectance respectively in a positive-polarity frame period; and a quantity represented by symbol  $V_o$  in Eq. (4) as the absolute value of said voltage appearing on said liquid crystal is set at the absolute value of said voltage appearing on said liquid crystal for a negative polarity for which said transmittance or said reflectance of said liquid-crystal display device is equal to about half said maximum transmittance or said maximum reflectance respectively in a negative-polarity frame period.

20. A method of driving an active-matrix liquid-crystal display device in accordance with claim 2 wherein: said fixed electric potential appearing on said positive-polarity data line in said hold period is set at a level higher than (V<sub>sp50</sub>-.DELTA.V<sub>ft</sub>) and said fixed electric potential appearing on said negative-polarity data line in said hold period is set at a level lower than (V<sub>sm50</sub>-.DELTA.V<sub>ft</sub>), where: symbol V<sub>sp50</sub> denotes an electric potential appearing on said positive-polarity data line as an electric potential corresponding to a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively among transmittance or reflectance values in a range of voltages appearing on said liquid crystal as voltages used in a display; symbol V<sub>sm50</sub> denotes an electric potential appearing on said negative-polarity data line as an electric potential corresponding to a tone showing a transmittance or a reflectance equal to about half a maximum transmittance or a maximum reflectance respectively among transmittance or reflectance values in said range of voltages appearing on said liquid crystal as voltages used in a display; and symbol .DELTA.V<sub>ft</sub> denotes a quantity expressed by Eq. (5) as follows: 18 V ft = [ V<sub>sp50</sub> + V<sub>sm50</sub> ) 2 ] - V<sub>com</sub> ( 5 )

### ***Conclusion***

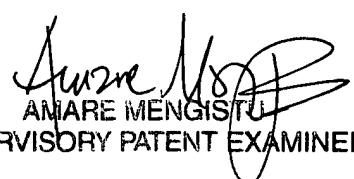
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta

January 16, 2008



AMARE MENGISTU  
SUPERVISORY PATENT EXAMINER